## Remarks

The Final Office Action dated February 3, 2011, indicates the following: claims 1, 3-10, 12 and 14-17 remain rejected under 35 U.S.C. § 103(a) over Tsuchi (US 2003/0160749) in view of Sakurai et al. (US 5,384,548); claims 11 and 13 remain rejected under 35 U.S.C. § 103(a) over the '749 reference in view of the '548 reference, and further in view of the Examiner's official notice; claim 2 remains rejected under 35 U.S.C. § 103(a) over the '749 reference in view of the '548 reference, and further in view of Nishimura (US 2001/0004255). In this discussion set forth below, Applicant traverses each rejection without acquiescing to any averment in the Office Action, unless Applicant expressly indicates otherwise.

Applicant renews arguments presented in Applicant's previous response, which for brevity are not repeated but are fully incorporated herein.

Each of the § 103(a) rejections fails because the Office Action has not established that the combination of the '749 and '548 references (upon which all rejections rely) teaches or suggests all claim limitations. For example, the Office Action does not assert that the references teach the claimed invention "as a whole" (§ 103(a)) including, *e.g.,* an input stage "configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant." The Examiner acknowledges that these aspects are not taught by the '759 reference (*see*, Final Office Action at page 3).

In an attempt to overcome this deficiency, the Examiner somehow relies upon the '548 reference, but fails to clearly articulate the rationale for the alleged combination. The record is uncontroverted that the rejections fail to explain that the '749 reference could be or would be modified to operate as taught by the '548 reference. The Examiner's response, reliant on equivalence, fails to clarify whether the Examiner proposes to: 1) replace the input stage of the primary '749 reference with the input stage of the secondary '548 reference, using the rationale of interchangeably equivalent elements, or 2) whether the Examiner uses the teachings of the secondary '548 reference to show a property is inherent in the primary '759 reference. In either case, as described below, the articulated rationale is not valid, and Applicant requests that the rejections be withdrawn.

Regarding the rationale for proposing to replace the input stage of the primary '749 reference with the input stage of the secondary '548 reference, the rejection fails because the Examiner has not shown that the cited embodiments are equivalent and because the '548 reference teaches away from using the cited embodiment. "In order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency must be recognized in the prior art, and cannot be based on applicant's disclosure or the mere fact that the components at issue are functional or mechanical equivalents." M.P.E.P. § 2144.06, *citing*, *In re Ruff*, 256 F.2d 590, 118 USPQ 340 (CCPA 1958). The only support provided for the Examiner's position on equivalence is that both embodiments include a PMOS pair and an NMOS pair. However, this conclusion ignores significant differences, including switches 111, 112, 113, 114, 115, 116, 117, 118, 119, and 120 included in the arrangement shown in FIG. 1 of the '749 reference. It should be apparent from a comparison of the figures that no combination of switching can cause the circuit of the '749 embodiment to be equivalent to that of the '548 embodiment.

The significance of the above differences is exemplified by the fact that the references teach away from using the cited embodiment of the secondary '548 reference. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). For example, the cited FIG. 1 of the secondary '548 reference is described therein as prior art exhibiting undesirable performance (*see, e.g.*, Background, describing the transconductance as being constant for only a small region of the common mode). The Office Action fails to explain why a skilled artisan would ignore the entirety of the '548 reference (including solutions that are the subject of the patent) to modify the primary '749 reference with the embodiment shown in FIG. 1 of the '548 reference. For the above reasons, this rationale fails to provide valid support for the rejection.

Regarding the rationale of inherency, the rejection is improper because it fails to explain that such aspects are necessarily present in the '749 reference to support the rejection. As discussed above, there are significant differences between FIG. 1 of the '548 reference and FIG. 1 of the '749 reference, in which no operation of the circuits causes the circuits to be equivalent. Because these circuits are not equivalent, transconductance behavior exhibited by the '548 embodiment would not necessarily be exhibited by the embodiment of the primary '749 reference. Therefore, it is not proper to rely upon the teachings of the '548 reference to support an inherency argument. Accordingly, the inherency rationale does not provide valid support for the rejections.

Accordingly, whether the Examiner relies on a rationale of interchangeably equivalent elements, or on a rationale of inherency, the § 103 rejections fail.

Regarding the rejections of claim 2 and other various dependent claims, such as those relating to the operation of switches to control a transconductance ratio, the rejections fail to establish that the various switching connectivity would be configured to maintain such a ratio constant in accordance with the claimed invention (as a whole).

Specific to claim 2, it remains unclear how the cited portion of the '255 reference (allegedly disclosing "using gamma corrected picture signals") is related to aspects directed to switches that operate based upon the presence of positive or negative gamma data as alleged in Examiner's response. Because the rejection fails to explain how the cited portion relates to switching, the rejection is improper and should be removed.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney/agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170 (or the undersigned).

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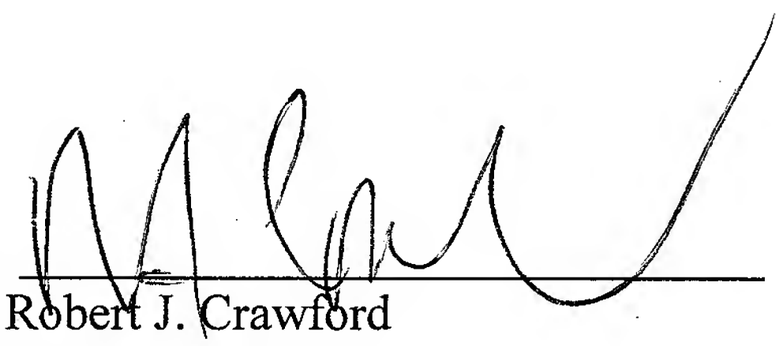
By: 

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